L Number	Hits	Search Text	DB	Time stamp
14	31	iss and (cycle periodic) and interrupt adj request and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 16:37
18	1131	instruction adj set and (cycle periodic) and interrupt adj request and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 16:37
19	3	instruction adj set adj simulat$ and (cycle periodic) and interrupt adj request and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 16:40
20	1	instruction adj set adj simulat$ and (cycle periodic) near request and interrupt adj request and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 16:40
-	158	703/4 and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 14:36
-	54	703/4 and (hardware) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 14:47
-	18	703/4 and hardware and processor and bus and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 14:48
-	11	703/4 and (model$ simulat$ emulat$) with bus and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 14:49
-	3	703/4 and (model$ simulat$ emulat$) near2 bus and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 14:54
-	46	703/13 and (model$ simulat$ emulat$) near2 bus and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 14:55

-	45	703/13 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:14
-	2	6002861.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:10
-	2	5812414.pn.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:11
-	40	703/13 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (coverifi$ verif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:16
-	3	703/13 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and coverifi$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:17
-	2	703/13 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and co-verifi$ and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:18
-	4	703/13 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:19
-	5	703/14 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:20
-	4	703/15 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:21
-	0	703/4 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:21
-	3	703/16 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:21

-	3	703/17 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:21
-	0	703/18 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:22
-	5	703/19 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:23
-	3	703/20 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:23
-	4	703/21 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:23
-	3	703/22 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:23
-	4	703/23 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:23
-	1	703/24 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:24
-	1	703/25 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:24
-	12	703/$ and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:26
-	5	716/4 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:26

-	3	716/5 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:26
-	3	716/6 and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:27
-	10	716/$ and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:27
-	7	714/$ and (model$ simulat$ emulat$) near2 bus and (hardware processor) and (co-verif$ coverif$) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/20 15:27
-	0	integrated adj circuit and hardware adj model and bus adj functional adj model and disabl$ near2 processor and (simulat$ emulat$ model) near2 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:31
-	0	((integrated adj circuit) (hardware adj model)) and bus adj functional adj model and disabl$ near2 processor and (simulat$ emulat$ model) near2 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:31
-	0	(integrated adj circuit) and ((hardware adj model) (bus adj functional adj model)) and disabl$ near2 processor and (simulat$ emulat$ model) near2 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:29
-	81	((integrated adj circuit) (hardware adj model) (bus adj functional adj model)) and disabl$ near2 processor and (simulat$ emulat$ model) near2 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:34
-	0	(integrated adj circuit) and ((hardware adj model) (bus adj functional adj model)) and disabl$ near4 processor and (simulat$ emulat$ model) near4 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:29
-	0	integrated adj circuit and hardware adj model and bus adj functional adj model and disabl$ with processor and (simulat$ emulat$ model) with processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:29
-	1	(integrated adj circuit) and ((hardware adj model) (bus adj functional adj model)) and disabl$ with processor and (simulat$ emulat$ model) with processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:30

-	0	((integrated adj circuit) (hardware adj model)) and bus adj functional adj model and disabl$ near4 processor and (simulat$ emulat$ model) near4 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:31
-	0	((integrated adj circuit) (hardware adj model)) and bus adj functional adj model and disabl$ with processor and (simulat$ emulat$ model) with processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:32
-	2	((integrated adj circuit) (hardware adj model) (bus adj functional adj model)) same disabl$ near2 processor and (simulat$ emulat$ model) near2 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:34
-	147	((integrated adj circuit) (hardware adj model) (bus adj functional adj model)) same (disabl$ simulat$ emulat$ model) near2 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:35
-	0	((integrated adj circuit) (hardware adj model) (bus adj functional adj model)) same (disabl$ and (simulat$ emulat$ model)) near2 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:36
-	0	(disabl$ and (simulat$ emulat$ model)) near2 processor same (simulat$ emulat$ model) near2 (bus integrated adj circuit) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:47
-	15	(disabl$ and (simulat$ emulat$ model)) near2 processor and (simulat$ emulat$ model) near2 (bus integrated adj circuit) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:49
-	116	(disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:50
-	215	(disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit microcomputer microprocessor microcontroller) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:51
-	48	((integrated adj circuit) (hardware adj model) (bus adj model)) and (disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:51
-	77	((integrated adj circuit) (hardware adj model) (bus adj model)) and (disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit microcomputer microprocessor microcontroller) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:55

-	0	((integrated adj circuit) and (hardware adj model) and (bus adj model)) and (disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:51
-	0	((integrated adj circuit) and (hardware adj model) and (bus adj model)) and (disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit microcomputer microprocessor microcontroller) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:52
-	5	instruction adj set adj simulator and ((integrated adj circuit) (hardware adj model) (bus adj model)) and (disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit microcomputer microprocessor microcontroller) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:58
-	77	((instruction adj set adj simulator) (integrated adj circuit) (hardware adj model) (bus adj model)) and (disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit microcomputer microprocessor microcontroller) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 09:59
-	1	((instruction adj set adj simulator) (integrated adj circuit) (hardware adj model)) and (bus adj model) and (disabl$ simulat$ emulat$ model$) near2 processor same (simulat$ emulat$ model$) near2 (bus integrated adj circuit microcomputer microprocessor microcontroller) and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:08
-	686	703/13 and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:09
-	0	703/13 and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (disabl$ inactive) near3 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:15
-	0	703/14 and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (disabl$ inactive) near3 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:14
-	0	703/15 and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (disabl$ inactive) near3 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:15
-	0	703/$ and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (disabl$ inactive) near3 processor and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:15

-	4	703/13 and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:15
-	3	703/14 and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:15
-	1	703/15 and (integrated adj circuit microprocessor microcontroller) and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:16
-	0	703/15 and (integrated adj circuit microprocessor microcontroller) and (instruction adj set adj simulat$) and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:16
-	0	703/15 and (integrated adj circuit microprocessor microcontroller) and (instruction adj set adj simulat$ iss) and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:16
-	1	703/14 and (integrated adj circuit microprocessor microcontroller) and (instruction adj set adj simulat$ iss) and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:17
-	3	703/13 and (integrated adj circuit microprocessor microcontroller) and (instruction adj set adj simulat$ iss) and (bus near model$) with hardware and (@ad<19990813 @rlad<19990813)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/23 10:17

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1 **Verifying IP-core based system-on-chip designs**
Chauhan, P.; Clarke, E.M.; Lu, Y.; Wang, D.;
ASIC/SOC Conference, 1999. Proceedings. Twelfth Annual IEEE International , 15-18 Sept. 1999
Pages:27 - 31

[Abstract] [PDF Full-Text (304 KB)] **IEEE CNF**

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2 **Symbolic model checking in practice**
Campos, S.V.A.;
Integrated Circuits and Systems Design, 1999. Proceedings. XII Symposium on , 29 Sept.-2 Oct. 1999
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[Abstract] [PDF Full-Text (44 KB)] **IEEE CNF**

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3 **Implementation of a PCI bus virtual driver using PLI, named pipes, and signals**
Hahn, D.; Russack, J.;
Verilog HDL Conference, 1997., IEEE International , 31 March-2 April 1997
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[Abstract] [PDF Full-Text (328 KB)] **IEEE CNF**

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4 **Interconnect modeling using integrated time-domain and frequency-domain techniques**
Hong You; Chune-Sin Yeh; Gadepally, B.;
WESCON/'95. Conference record. 'Microelectronics Communications Technology Producing Quality Products Mobile and Portable Power Emerging Technologies' , 7-9 Nov. 1995
Pages:88

[Abstract] [PDF Full-Text (368 KB)] **IEEE CNF**

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5 **System level verification of ASIC chip-sets**
Tayal, S.; Moezzi, A.; Magnusson, E.;
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International , 27 Sept.-1 Oct. 1993
Pages:283 - 287

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

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6 **Overview of PowerPC 620 multiprocessor verification strategy**
Jen-Tien Yen; Sullivan, M.; Montemayor, C.; Wilson, P.; Evers, R.;
Test Conference, 1995. Proceedings., International , 21-25 Oct. 1995
Pages:167 - 174

[Abstract] [PDF Full-Text (736 KB)] **IEEE CNF**

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1 Embedded hardware design case studies: Design flow for HW / SW acceleration transparency in the thumbpod secure embedded system 80%

David Hwang , Bo-Cheng Lai , Patrick Schaumont , Kazuo Sakiyama , Yi Fan , Shenglin Yang , Alireza Hodjat , Ingrid Verbauwhede

Proceedings of the 40th conference on Design automation June 2003

This paper describes a case study and design flow of a secure embedded system called ThumbPod, which uses cryptographic and biometric signal processing acceleration. It presents the concept of HW/SW acceleration transparency, a systematic method to accelerate Java functions in both software and hardware. An example of acceleration transparency for a Rijndael encryption function is presented. The embedded prototype hardware platform is also described. Acceleration transparency yields software and ...

2 Am embedded system case study: the firm ware development environment for a multimedia audio processor 80%

Clifford Liem , Marco Cornero , Miguel Santana , Pierre Paulin , Ahmed Jerraya , Jean-Marc Gentit , Jean Lopez , Xavier Figari , Laurent Bergher

Proceedings of the 34th annual conference on Design automation conference June 1997

3 The A to Z of SoCs 77%

Reinaldo A. Bergamaschi , John Cohn

Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design November 2002

The exploding complexity of new chips and the ever decreasing time-to-market window are forcing fundamental changes in the way systems are designed. The advent of Systems-on-Chip (SoC) based on pre-designed intellectual-property (IP) cores has become an absolute necessity for embedded systems companies to remain competitive. Designing an SoC, however, is extremely complex, as it encompasses a range of difficult problems in hardware and software design. This paper explains a wide range of SoC iss ...

4 Multi-sim, a dynamic multi-level simulator 77%

Robert C. Chen , James E. Coffman

Proceedings of the no 15 design automation conference on Design automation June 1978

This paper describes an approach to efficient logic simulation of microprocessor based systems using automatic, dynamic switching of level of simulation.

5 Highlights of ISSCC: high-speed heterogenous design techniques: A reconfigurable signal processing IC with embedded FPGA and multi-port flash memory 77%

M. Borgatti , L. Calì , G. De Sandre , B. Forêt , D. Iezzi , F. Lertora , G. Muzzi , M. Pasotti , M. Poles , P. L. Rolandi

Proceedings of the 40th c nference on Design aut mation June 2003

A 1GOPS dynamically reconfigurable processing unit with embedded Flash memory and SRAM-based FPGA targets image-voice processing and recognition applications. Code, data and FPGA bitstreams are stored in the embedded Flash memory and are independently accessible through 3 content-specific, 64-bit I/O ports with a peak read rate of 1.2GB/s. The system is implemented in a 0.18um, 2PL-6ML CMOS Flash technology, chip area is 70mm2.

6 Partitioned instruction cache architecture for energy efficiency 77%

Soontae Kim , N. Vijaykrishnan , Mahmut Kandemir , Anand Sivasubramaniam , Mary Jane Irwin

ACM Transactions on Embedded Computing Systems (TECS) May 2003

Volume 2 Issue 2

The demand for high-performance architectures and powerful battery-operated mobile devices has accentuated the need for low-power systems. In many media and embedded applications, the memory system can consume more than 50% of the overall system energy, making it a ripe candidate for optimization. To address this increasingly important problem, this article studies energy-efficient cache architectures in the memory hierarchy that can have a significant impact on the overall system energy ...

7 Simulation and verification: Validation in a component-based design flow for multicore SoCs 77%

Gabriela Nicolescu , Sungjoo Yoo , Aimen Bouchhima , Ahmed Amine Jerraya

Proceedings of the 15th international symposium on System Synthesis October 2002

Currently, since many SoCs include heterogeneous components such as CPUs, DSPs, ASICs, memories, buses, etc., system integration becomes a major step in the design flow. To enable this integration, we use a design approach called component based-design approach. In this approach, the validation of system integration takes most of design efforts. This paper presents an automatic method of SoCs design validation. Based on a generic simulation wrapper architecture, the presented method provides aut ...

8 System level modeling and verification: Instruction-based system-level power evaluation of system-on-a-chip peripheral cores 77%

Tony D. Givargis , Frank Vahid , Jörg Henkel

Proceedings of the 13th international symposium on System synthesis September 2000

Various system-level core-based power evaluation approaches for core types like microprocessors, caches, main memories, and buses, have been proposed in the past. Approaches for other types of components have been based either on the gate-level, register-transfer level, or behavioral-level. We propose a new technique, suitable for a variety of cores like peripheral cores, that is the first to combine gate-level power data with a system-level simulation model written in C++ or Java. For that purp ...

9 Formal Aspects and Distributed Systems: Accelerating boolean satisfiability through application specific processing 77%

Ying Zhao , Sharad Malik , Matthew Moskewicz , Conor Madigan

Proceedings of the 14th international symposium on Systems synthesis September 2001

This paper presents our work in developing an application specific multiprocessor system for SAT, utilizing the most recent results such as the development of highly efficient sequential SAT algorithms, the emergence of commercial configurable processor cores and the rapid progress in IC manufacturing techniques. Based on an analysis of the basic SAT search algorithm, we propose a new parallel SAT algorithm that utilizes fine grain parallelism. This is then used to design a multiprocessor archit ...

10 The case for a configure-and-execute paradigm 77%

Frank Vahid , Tony Givargis
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Proceedings of the 35th annual conference on Design automation conference May 1998
The difficulty of emb edded system co-design is increasing rapidly due to the incr easing complexity of individual parts, the variety of parts available and pr essure to use multiple processors to me et performanc e criteria. V alidation tools should contain sever al features in order to keep up with this trend, including the ability to dynamically change detail levels, built in protection for intellectual property, and supp ort for gradual migr ation of functionalityfrom a simulati ...

13 The case for a single-chip multiprocessor 77%
Kunle Olukotun , Basem A. Nayfeh , Lance Hammond , Ken Wilson , Kunyung Chang
Proceedings of the seventh international conference on Architectural support for programming languages and operating systems September 1996
Volume 31 , 30 Issue 9 , 5
Advances in IC processing allow for more microprocessor design options. The increasing gate density and cost of wires in advanced integrated circuit technologies require that we look for new ways to use their capabilities effectively. This paper shows that in advanced technologies it is possible to implement a single-chip multiprocessor in the same area as a wide issue superscalar processor. We find that for applications with little parallelism the performance of the two microarchitectures is co ...

14 Evaluation of design alternatives for a multiprocessor microprocessor 77%
Basem A. Nayfeh , Lance Hammond , Kunle Olukotun
ACM SIGARCH Computer Architecture News , Proceedings of the 23rd annual international symposium on Computer architecture May 1996
Volume 24 Issue 2
In the future, advanced integrated circuit processing and packaging technology will allow for several design options for multiprocessor microprocessors. In this paper we consider three architectures: shared-primary cache, shared-secondary cache, and shared-memory. We evaluate these three architectures using a complete system simulation environment which models the CPU, memory hierarchy and I/O devices in sufficient detail to boot and run a commercial operating system. Within our simulation envir ...

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